ES8318

Low Power Mono Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM master or slave serial data port
- 256/384Fs and USB 12/24 MHz
- I^2C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 103 dB signal to noise ratio, -90 dB THD+N
- Two single ended analog input mux or differential analog input
- Low noise pre-amplifier
- Auto level control (ALC) and noise gate
- Support analog and digital microphone

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 112 dB signal to noise ratio, -85 dB THD+N
- One pair of analog output with headphone driver and differential output option
- Pop and click noise suppression

Low Power

- 1.8V to 3.3V operation
- Low standby current

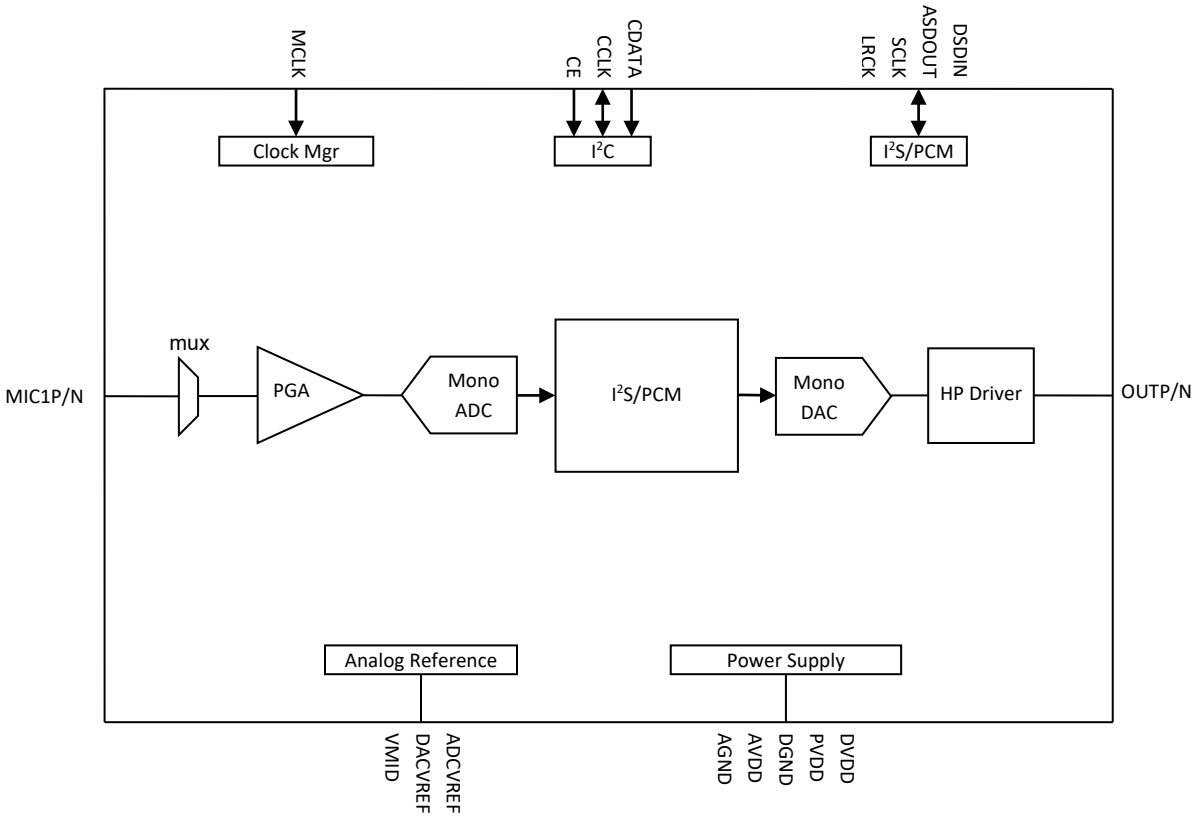
APPLICATIONS

- Automotive
- Phone
- Toy
- 2-way radio
- Dash cam
- IP Camera
- DVR, NVR
- Surveillance

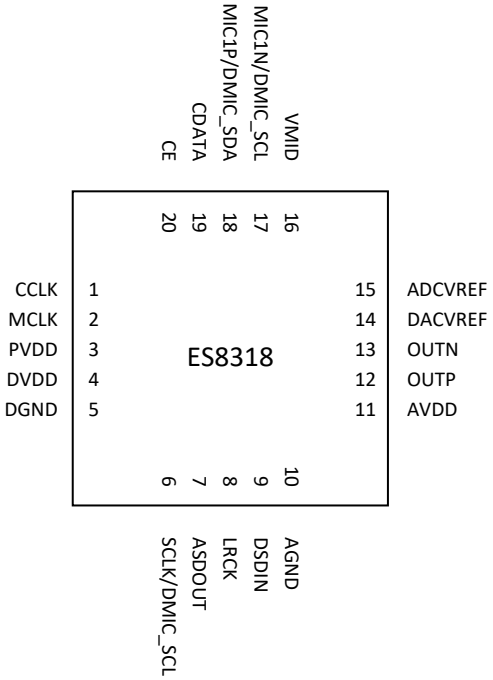
ORDERING INFORMATION

ES8318 -40°C ~ +125°C
QFN-20

1. BLOCK DIAGRAM



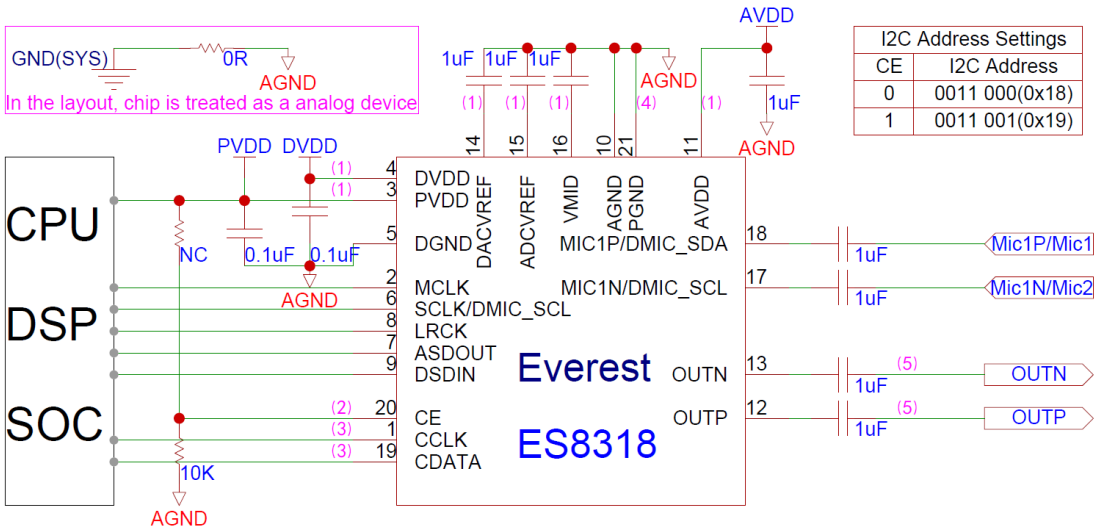
2. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA, CE	1, 19, 20	I, I/O, I	I^2C clock, data, address
MCLK	2	I	Master clock
SCLK/DMIC_SCL	6	I/O	Serial data bit clock or DMIC clock in master mode
LRCK	8	I/O	Serial data left and right channel frame clock
ASDOUT	7	O	ADC serial data output
DSDIN	9	I	DAC serial data input
MIC1P/DMIC_SDA MIC1N/DMIC_SCL	18 17	I I/O	Mic input/DMIC data and clock
OUTP, OUTN	12, 13	O	Differential analog output
PVDD	3	Analog	Power supply for the digital input and output
DVDD, DGND	4, 5	Analog	Digital power supply
AVDD, AGND	11, 10	Analog	Analog power supply
VMID	16	Analog	Filtering capacitor connection
ADCVREF, DACVREF	15, 14	Analog	Filtering capacitor connection
PGND	21	Analog	Package ground

3. TYPICAL APPLICATION CIRCUIT

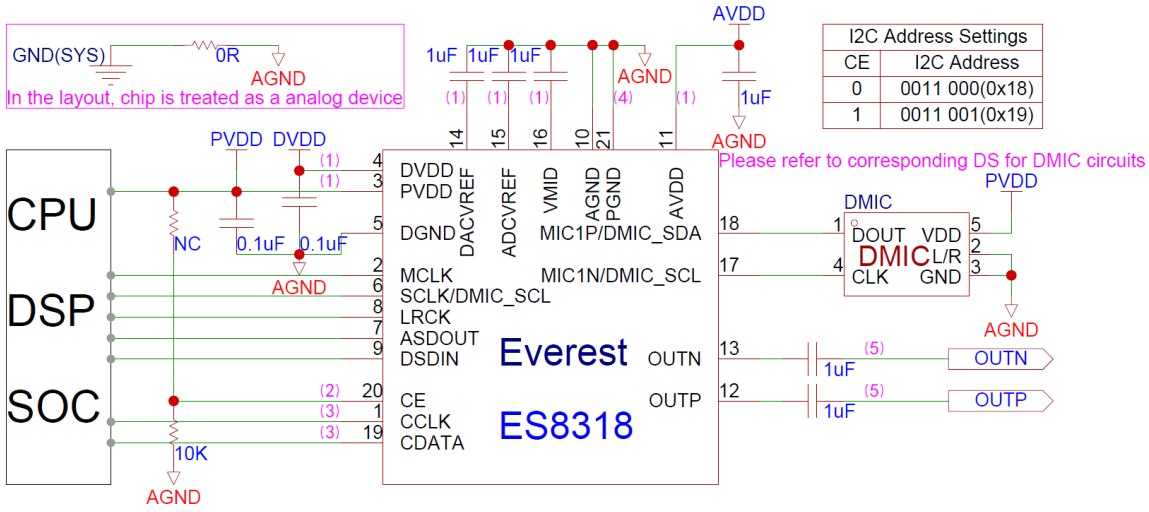
ANALOG INPUT:



I2C Address Settings	
CE	I2C Address
0	0011 000(0x18)
1	0011 001(0x19)

(1) For optimal performance, the filter capacitor should be placed on the same layer and as close as possible to the pin it is filtering
(2) Each address pin(CE) must be tied to either PVDD(logic high) or AGND (logic low) using an external resistor
(3) Reservation(预留) of RC filter circuit in the I2C signal path are recommended in case I2C signal integrity are not ideal(理想)
(4) PIN21:PGND(on the underside of the chip)must be electrically tied to the ground
(5) External RC filter can be added if lower out of band noise are needed

DMIC INPUT:



I2C Address Settings	
CE	I2C Address
0	0011 000(0x18)
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(3) Reservation(预留) of RC filter circuit in the I2C signal path are recommended in case I2C signal integrity are not ideal(理想)
(4) PIN21:PGND(on the underside of the chip)must be electrically tied to the ground
(5) External RC filter can be added if lower out of band noise are needed

4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc.) and USB clocks (12/24 MHz).

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 0011 00x, where x equals CE (input pin: 1 being connected to supply and 0 being connected to ground). The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^2C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	0011 00 CE	0	ACK	RAM	ACK	DATA	ACK	Stop

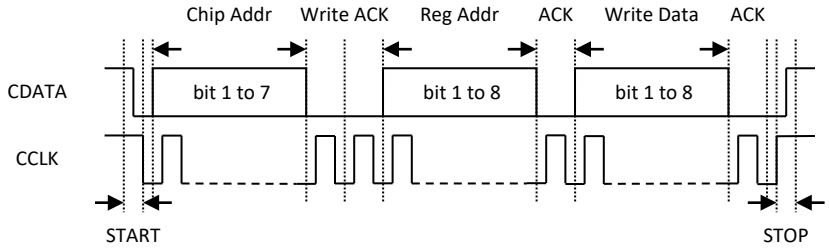


Figure 1a I²C Write Timing

Table 2 Read Data from Register in I²C Interface Mode

	Chip Address	R/W		Register Address		
Start	0011 00 CE	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	0011 00 CE	1	ACK	Data	NACK	Stop

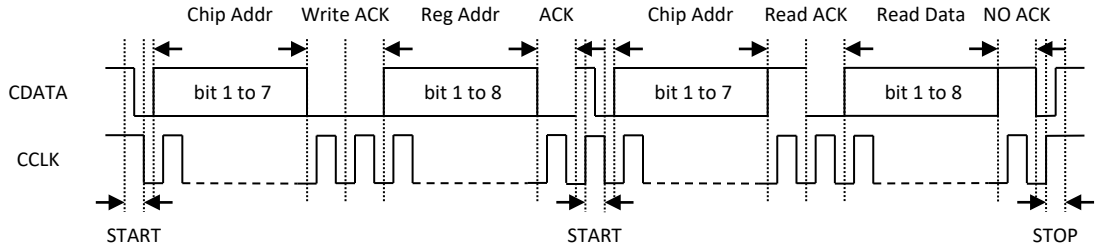


Figure 1b I²C Read Timing

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and DSDIN or ASDOUT pins. These formats are I^2S, left justified, right justified and DSP/PCM. DAC input DSDIN is sampled by the device on the rising edge of SCLK. ADC data is out at ASDOUT on the falling edge of SCLK. The relationship of SDATA (DSIN/ASDOUT), SCLK and LRCK with these formats are shown through Figure 2a to Figure 2d. In loop back mode, DSDIN input data are routed to ASDOUT output data.

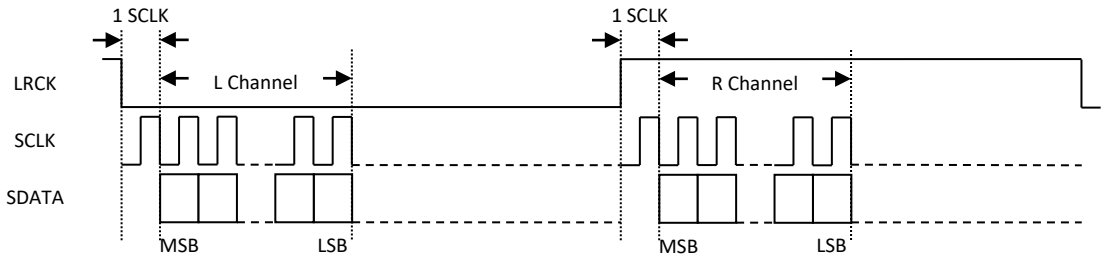


Figure 2a I^2S Serial Audio Data Format

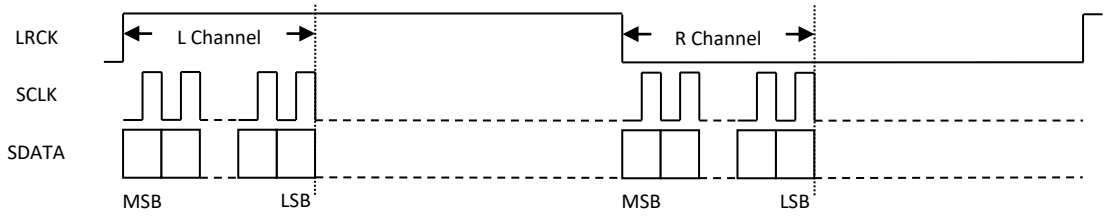


Figure 2b Left Justified Serial Audio Data Format

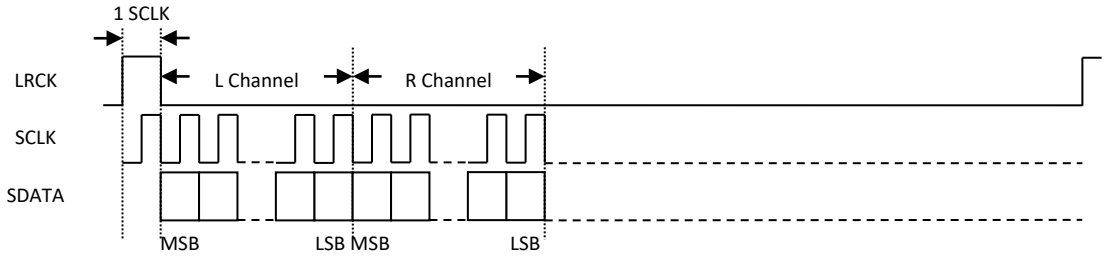


Figure 2c DSP/PCM Mode A Serial Audio Data Format

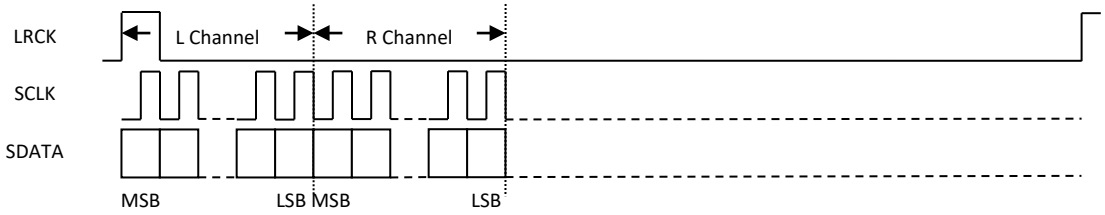


Figure 2d DSP/PCM Mode B Serial Audio Data Format

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+125°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
DVDD	1.62	1.8/3.3	3.6	V
PVDD	1.62	1.8/3.3	3.6	V
AVDD	1.71	1.8/3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	100	103	105	dB
THD+N	-95	-90	-85	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input (differential P and N)		2.2*AVDD/3.3		Vrms
Input Impedance		6		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	110	112	114	dB
THD+N	-95	-90	-85	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Analog Output				
Full Scale Output (differential P and N)	1.8*AVDD/3.3	1.9*AVDD/3.3	1.99*AVDD/3.3	Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V		10		mA
Power Down Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=3.3V		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			100	KHz
LRCK duty cycle (Note 1)		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to SDOUT valid DVDD=3.3V DVDD=1.8V	T_{SDO}		16 39	ns
LRCK edge to SDOUT valid (Note 2) DVDD=3.3V DVDD=1.8V	T_{LDO}		11 25	ns
SDIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to SDIN hold time	T_{SDIH}	10		ns

Note 1: one SCLK period of high time in DSP/PCM modes.

Note 2: only apply to MSB of Left Justified or DSP/PCM mode B.

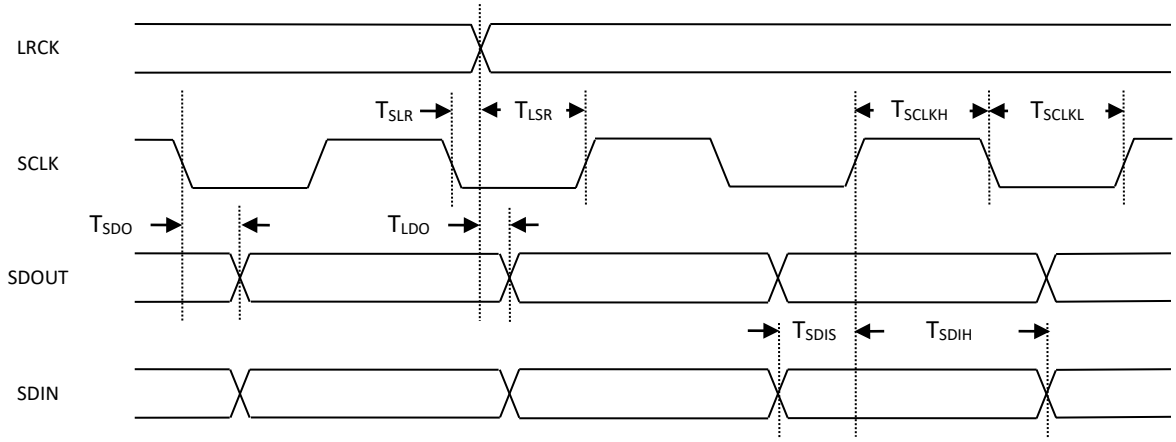


Figure 3 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

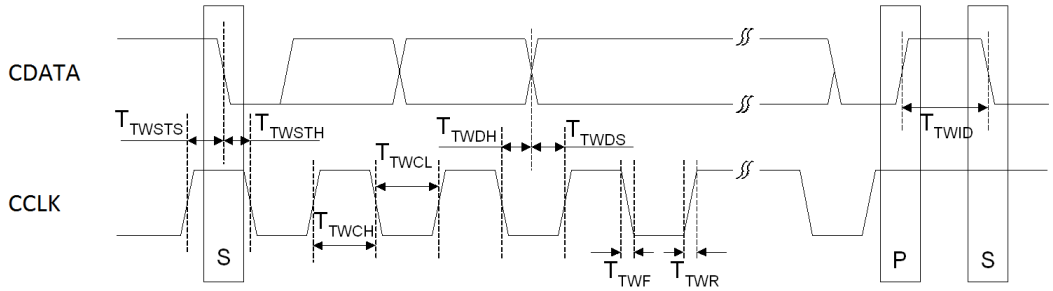
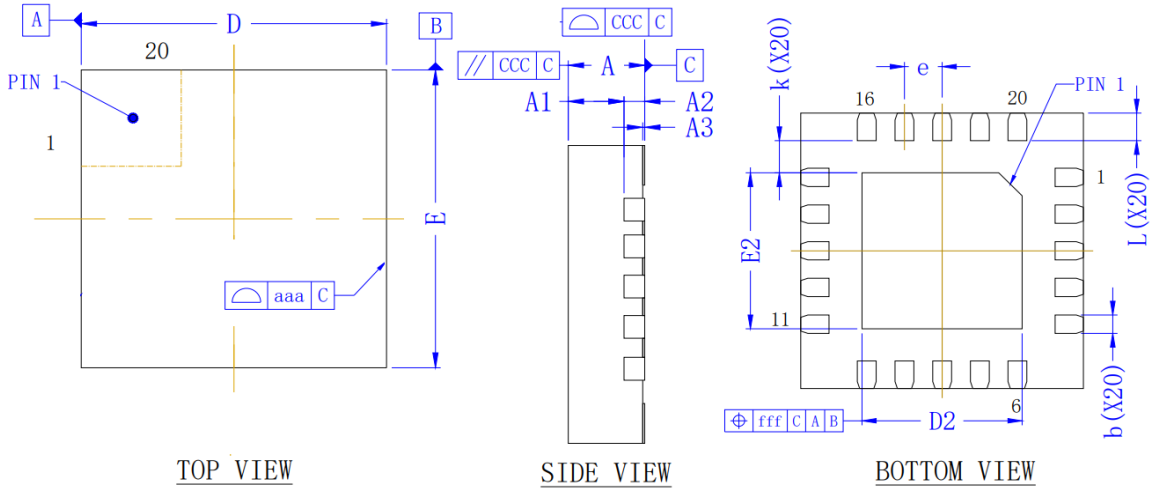


Figure 4 I²C Timing

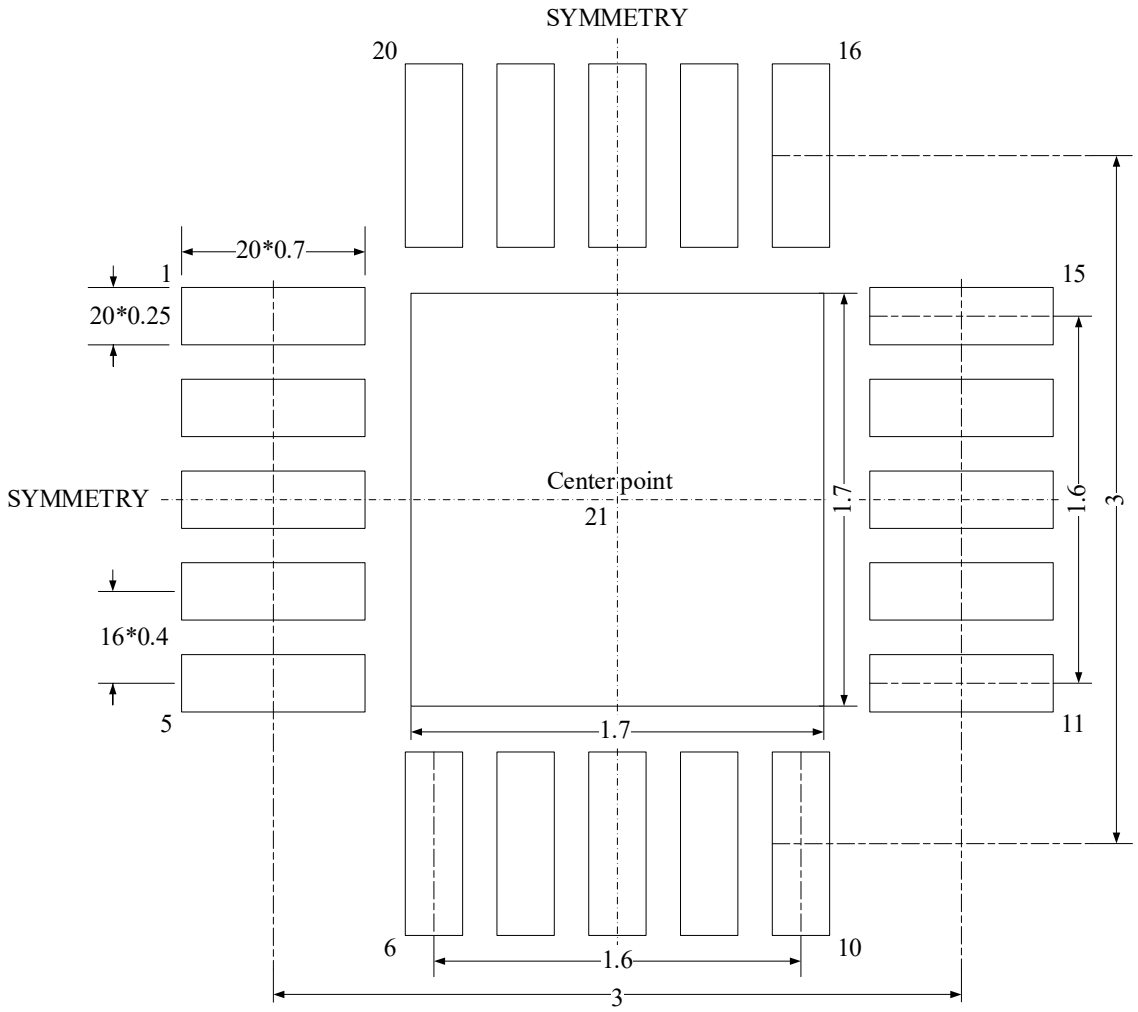
8. PACKAGE (UNIT: MM)

QFN-20L-3X3(P0.4T0.55) Package Outline Drawing



Item	Symbol	Minimum	Normal	Maximum
Total Thickness	A	0.50	0.55	0.60
Stand Off	A1	0.00	0.02	0.05
Molding Thickness	A2	---	0.40	---
LF Thickness	A3	0.152 REF		
Lead Width	b	0.15	0.20	0.25
Body Size	D	3 BSC		
	E	3 BSC		
Lead Pitch	e	0.4 BSC		
Exposed Pad Size	D2	1.60	1.70	1.80
	E2	1.60	1.70	1.80
Lead Length	L	0.20	0.30	0.40
Lead tip to Exposed Pad	K	0.35 REF		
Package Edge Tolerance	aaa	0.1		
Molding Flatness	ccc	0.1		
Coplanarity	eee	0.08		
Lead Offset	bbb	0.1		
Exposed Pad Offset	fff	0.1		

9. LAND PATTERN



NOTES:
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. Drawing is not to scale.
3. This drawing is subject to change without notice.
4 .The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

10.CORPORATE INFORMATION

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Email: info@everest-semi.com

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